IN THE CLAIMS

1. An integrated circuit with a jitter measurement circuit, comprising:

a plurality of delay elements, each delay element having an associated delay, an input configured to receive an input clock signal and an output responsive to the associated delay and the input clock signal, wherein the input clock signal has a significant instant;

a first set of circuitry connected to the inputs and outputs of the plurality of delay elements, said first set of circuitry configured to detect the significant instant on the input clock signal, the first set of circuitry further configured to output a signal responsive to the significant instant on the input clock signal; and

a second set of circuitry configured to receive the signal responsive to the significant instant on the input clock signal and a first trigger signal, the second set of circuitry further configured to latch onto the signal responsive to the significant instant on the input clock signal and further responsive to a significant instant on the first trigger signal, wherein a measure for jitter is determined from the latched signal responsive to the significant instant on the input clock signal.

2. The integrated circuit of claim 1, wherein the associated delay of each delay element is approximately equal.

3. The integrated circuit of claim 1, wherein the plurality of delay elements are serially connected together.

4. The integrated circuit of claim 1, wherein the associated delay of each delay element is controlled by a delay control circuit.

5. The integrated circuit of claim 4, wherein the delay control circuit is a charge pump controlled delay lock loop.

6. The integrated circuit of claim 1, wherein the first set of circuitry includes a plurality of two-input logic gates, each of the plurality of two-input logic gate corresponding to each of the plurality of delay elements.

7. The integrated circuit of claim 6, wherein the inputs of the plurality of two-input logic gates is coupled to the input and the output of one of the plurality of delay elements.

8. The integrated circuit of claim 7, wherein one of the inputs of each of the plurality of two-input logic gates is coupled by means of an inverter logic gate.

9. The integrated circuit of claim 7, wherein one of the inputs of each of the plurality of two-input logic gates is coupled by means of wired connection.

10. The integrated circuit of claim 6, wherein each of the plurality of two-input logic gates is capable of producing a signal responsive to the significant instant on the input clock signal.

11. The integrated circuit of claim 1, wherein the second set of circuitry includes a first plurality of latching circuits, each of the first plurality of latching circuits corresponding to each of the plurality of delay elements.

12. The integrated circuit of claim 1, wherein the input clock signal is related to a reference clock signal.

13. The integrated circuit of claim 12, wherein the trigger signal is delayed by a first predetermined delay from the reference clock signal.

14. The integrated circuit of claim 13, wherein the first predetermined delay is longer than the first delay.

15. The integrated circuit of claim 13, wherein a measure for jitter is determined by comparing the latched signal responsive to the significant instant on the input clock signal to the first predetermined delay.

16. The integrated circuit of claim 1, wherein the measure for jitter is filtered.

17. The integrated circuit of claim 16, wherein the measure of jitter is filtered by means of a single one detector.

18. The integrated circuit of claim 1, wherein the latched signal responsive to the significant instant on the input clock signal is recorded for a first number of significant instants on the first trigger signal.

19. The integrated circuit of claim 18, wherein the latched signal responsive to the significant instant on the input clock signal is recorded by a third set of circuitry.

20. The integrated circuit of claim 19, wherein the third set of circuitry includes a second plurality of latching circuits, each of the second plurality of latching circuits corresponding to each of the plurality of delay elements.

21. The integrated circuit of claim 20, wherein each of the second plurality of latching circuits is provided with logic circuitry in a feedback loop for recording the presence of a desired input to the second plurality of latching circuits.

22. The integrated circuit of claim 21, wherein the desired input to the second plurality of latching circuits is a logic level high.

23. The integrated circuit of claim 1, further comprising a result calculator configured to provide information collected from the measure of jitter.

24. The integrated circuit of claim 23, wherein the result calculator is configured to provide information of an earliest occurrence of the significant instant on the input clock signal.

25. The integrated circuit of claim 23, wherein the result calculator is configured to provide information of an latest occurrence of the significant instant on the input clock signal.

26. The integrated circuit of claim 23, wherein the result calculator is configured to provide information of a difference between an earliest and a latest occurrence of the significant instant on the input clock signal.

27. The integrated circuit of claim 23, wherein the result calculator is configured to provide information on an average of the significant instant on the input clock signal.

28. The integrated circuit of claim 23, wherein the result calculator is configured to provide information on a median of the significant instant on the input clock signal.

29. The integrated circuit of claim 23, wherein the result calculator is configured to provide information on a standard deviation of the significant instant on the input clock signal.

30. The integrated circuit of claim 23, wherein the result calculator is configured to provide information responsive to a mode selection signal.

31. A method for measuring jitter of a significant instant on a clock signal derived from a reference clock signal, comprising:

receiving an input clock signal, wherein the input clock signal has a significant instant;

delaying the input clock signal by a first delay to produce a delayed input clock signal and a delayed significant instant on the delayed input clock signal;

receiving a trigger signal, wherein the trigger signal is delayed from the reference clock signal by a second delay;

detecting the delayed significant instant on the delayed input clock signal; and

producing a jitter measurement signal responsive to the delayed significant instant on the delayed input clock signal and the trigger signal.

32. The method of claim 31, further comprising deriving a jitter measure through a comparison of the jitter measurement signal to the first delay.

33. The method of claim 31, further comprising filtering the jitter measurement signal to produce a filtered jitter measurement signal.

34. The method of claim 33, wherein the filtered jitter measurement signal contains information of an earliest occurrence of the delayed significant instant on the delayed input clock signal.

35. The method of claim 33, wherein the filtered jitter measurement signal contains information of a latest occurrence of the delayed significant instant on the delayed input clock signal.

36. The method of claim 31, further comprising recording the jitter measurement signal for a plurality of trigger signals.

37. The method of claim 36, further comprising determining an earliest occurrence of the significant instant.

38. The method of claim 36, further comprising determining a latest occurrence of the significant instant on the delayed input clock signal.

39. The method of claim 36, further comprising determining a difference between an earliest and latest occurrence of the significant instant on the delayed input clock signal.

40. The method of claim 36, further comprising determining a statistic of the significant instant on the delayed input clock signal.

41. The method of claim 31, wherein an associated frequency of the reference clock signal is adjusted responsive to the jitter measurement signal.

42. The method of claim 31, wherein the first delay is adjusted responsive to the jitter measurement signal.

43. The method of claim 31, wherein the second delay is adjusted responsive to the jitter measurement signal.

44. The method of claim 31, further comprising inputting the reference clock signal to a circuit to produce the input clock signal.

45. The method of claim 44, wherein the circuit is adjusted responsive to the jitter measurement signal.

46. A system responsive to jitter in the system, comprising:

a reference clock configured to generate a reference clock signal having an associated frequency;

a plurality of circuits configured to receive the reference clock signal and operative to generate an input clock signal, the plurality of circuits having a first set of characteristics; and

a jitter measurement sub-system configured to receive the reference clock signal and the input clock signal and operative to generate a jitter measurement output signal responsive to a significant instant of the input clock signal, wherein the jitter measurement sub-system includes:

a plurality of delay elements having a plurality of associated delays configured to generate a synthesized signal from the reference clock signal and the input clock signal; and

at least one programmable delay element having at least one associated programmable delay configured to produce a trigger signal for generating the jitter measurement output signal from the synthesized signal;

wherein the system is operative to adjust at least one parameter of the system responsive to the jitter measurement output signal.

47. The system of claim 46, wherein the at least one parameter of the system is at least one parameter of the jitter measurement sub-system.

48. The system of claim 46, wherein the at least one parameter includes the associated frequency.

49. The system of claim 46, wherein the reference clock signal further has an associated duty cycle, and the at least one parameter includes the associated duty cycle.

50. The system of claim 46, wherein the at least one parameter includes at least one characteristic from the first set of characteristics.

51. The system of claim 46, wherein the plurality of circuits includes a plurality of sub-circuits having a second set of characteristics, and wherein the at least one parameter includes at least characteristic from the second set of characteristics.

52. The system of claim 46, wherein each of the plurality of associated delays is equal.

53. The system of claim 46, wherein at least one of the plurality of associated delays is not equal to other of the plurality of associated delays.

54. The system of claim 46, wherein the at least one parameter includes at least one of the plurality of associated delays.

55. The system of claim 46, wherein the at least one parameter includes all of the plurality of associated delays.

56. The system of claim 46, wherein the at least one parameter includes the at least one associated programmable delay.